Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claim 1 (Canceled)

Claim 2 (Currently Amended): A system LSI according to claim 9 [[1]], wherein the first and second circuit blocks are tested on [[a]] the wafer before fabrication of the system LSI is completed.

Claims 3-4 (Canceled)

Claim 5 (Currently Amended): A system LSI according to claim 9 [[1]], further comprising:

~~a third circuit block; and~~

a switching circuit, connected [[both]] to the second circuit block and the first and second power supply lines, that couples either one of the first and second power supply lines to the second circuit block ~~terminals and to the third circuit block, wherein the switching circuit selectively connects the third circuit block to the first and second power supply terminals whereby the third circuit block is tested efficiently~~.

Claim 6 (Currently Amended): A system LSI according to claim 10 [[5]], wherein the first, second and third circuit blocks are tested on [[a]] the wafer before fabrication of the system LSI is completed.

Claims 7-8 (Canceled)

Claim 9 (New): A system large scale integration (LSI), comprising:

first, second and third circuit blocks, each circuit block being located on a wafer;

a first power supply terminal located on the wafer and supplied with a first power supply voltage for test, wherein the first power supply voltage has a first voltage level and has a second voltage level which is different from the first voltage level;

a first power supply line located on the wafer, which surrounds the first, second and third circuit blocks, and which is connected to the first power supply terminal and the first and second circuit blocks;

a second power supply terminal located on the wafer and supplied with a second power supply voltage for test, wherein the second power supply voltage has the first voltage level and has a third voltage level which is different from the first and second voltage levels; and

a second power supply line located on the wafer, which surrounds the first, second and third circuit blocks, and which is connected to the second power supply terminal and the third circuit block.

Claim 10 (New): A system LSI according to claim 9, wherein the first power supply line is surrounded by the second power supply line.

Claim 11 (New): A system LSI according to claim 5, wherein the first power supply line is surrounded by the second power supply line.